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Implementation of Modulation Techniques for Inverters

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Abstract: Multilevel inverter technology has emerged in recent times as a very important in the area of highpower medium-voltage energy control. In this paper, cascaded multilevel inverter is used to reduce the total harmonic distortion. A cascaded multilevel inverter consists of series Hbridge (single-phase, full-bridge) inverter units. Pulse Width Modulation (PWM) inverters play a major role in the field of power electronics. Space Vector Modulation (SVM) is the popular PWM method and possibly the best among all the PWM techniques as it generates higher voltages with low total harmonic distortion .This paper comprehensively analyzes the relationship between space-vector modulation and three-phase sine pulse width modualtion (PWM). The simulation is done by MATLAB Simulink software.

Keywords: Cascaded Multilevel Inverter, Sinepulse width modulation, Space- vector pulsewidth modulation.

I. INTRODUCTION

Multilevel converters present great advantages compared with typical and very well known two-level converters. These advantages are fundamentally focused on improvements in the output signals quality and a nominal power increase in the converter. These properties make multilevel converters very attractive to the industry and nowadays, researchers all over the world are spending great efforts trying to improve multilevel converters performance as the control simplification and the performance of different optimization algorithms in order to enhance the Total Harmonic Distortion (THD) of the output signals.

Plentiful multilevel converter topologies have been proposed during the last two decades. In this paper we have discussed mainly three different major multilevel converter structures: cascaded H-bridges converter, diode clamped and flying capacitors. Moreover, abundant modulation techniques and control paradigms have been developed for multilevelconverters but main focus of the thesis is around sinusoidal pulse width modulation (SPWM) and space vector modulation(SVM).

II. MULTILEVEL INVERTERS

A. General

Multilevel inverter is divide the main dc supply voltage into several smaller dc sources which are used to synthesize an ac voltage into staircase, or stepped, approximation of the desired sinusoidal waveform. A waveform generated with five dc-sources each with one-volt magnitude approximates the desired sinusoid, as shown in figure 1. The five dc sources (five steps) produce a peak to peak voltage of 10 volts using 11 discrete levels. Figure 1 illustrates an example multilevel waveform. Using multiple levels, the multilevel inverter can yield operating characteristics such a high voltages, high power levels, and high efficiency without the use of transformers.

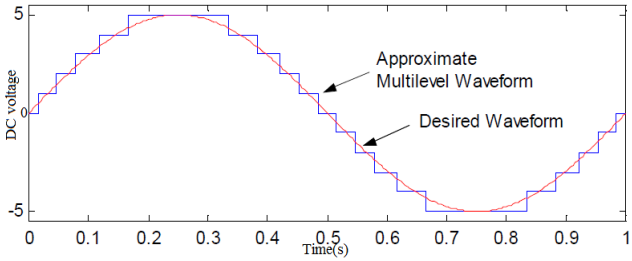

Fig1 Example multilevel sinusoidal approximation using 11-Levels

The multilevel inverter combines individual dc sources at specified times to yield a sinusoidal resemblance; by using more steps to synthesize the sinusoidal waveform, the waveform approaches the desired sinusoid and the total harmonic distortion approaches zero.

B. Types Of Multilevel Inverter

There are three main types of multilevel inverter: (1) diode-clamped inverter, (2) capacitor-clamped inverter, and (3) Cascaded inverter. The multilevel inverter may be implemented at the discrete component level dividing the main dc supply voltage into smaller voltages.

C. Cascade H-Bridge Inverter

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2n+1, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages

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of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types.

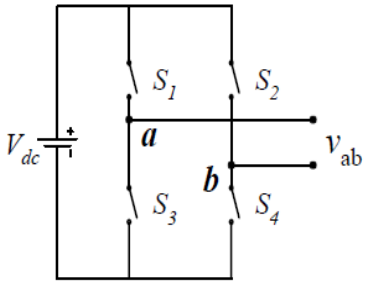

Fig. 2 Single H-bridge configuration

An n level cascaded H-bridge multilevel inverter needs 2(n-1) switching devices where n is the number of the output voltage level. The four switches S1, S2, S3 and S4 controlled to generate three discrete outputs Vab with levels of –Vdc, 0, +Vdc. When S2 and S3 are on the output is –Vdc; When either pair S1 and S2 or S3 and S4 are on the output is 0; when S1 and S4 are turned on the output is +Vdc .

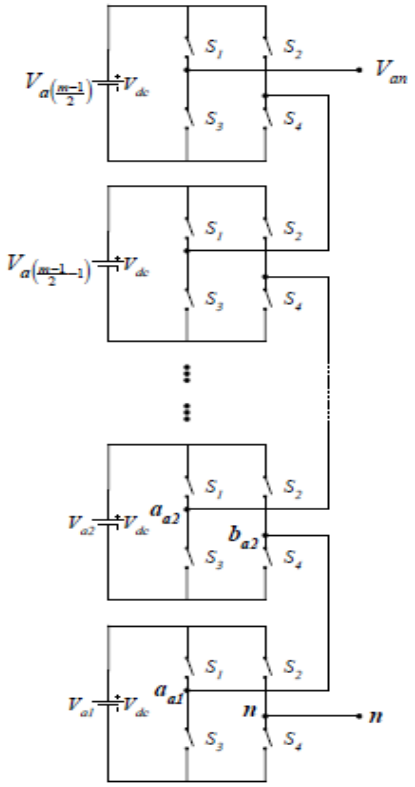

Fig. 3. Cascaded H-bridge multilevel inverter

Advantages of cascade multilevel H-bridge inverter with s separate dc source per phase are as follows

1. The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.
2. Switching redundancy for inner voltage levels is possible because the phase voltage output is sum of each bridge's output.
3. Potential of electrical shock is reduced due to the separate dc sources or voltage balancing capacitors
4. Requires the least number of components considering there are no extra clamping diodes are voltages balancing

III. MODULATION TECHNIQUES

Mainly the power electronic converters are operated in the "switched mode". Which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off). This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM), since the desired average value is controlled by modulating the width of the pulses.

A. PWM Techniques

The fundamental methods of pulse-width modulation (PWM) are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. A sample PWM method is described below.

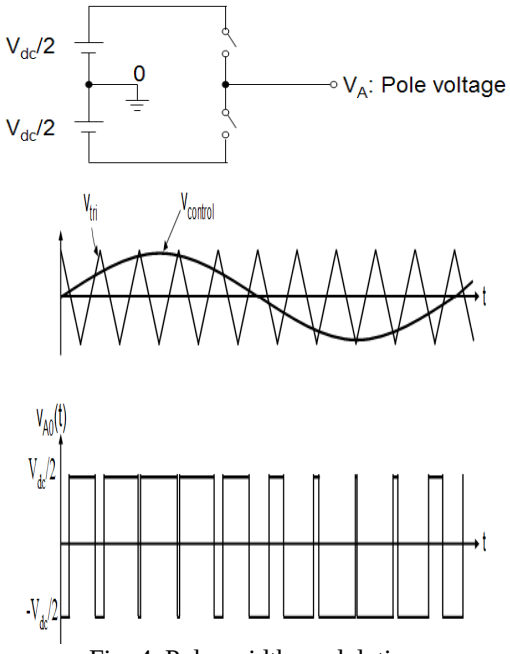

Fig. 4. Pulse width modulation

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Different PWM techniques applicable to inverters are:

1. Single-pulse modulation
2. Multiple-pulse modulation
3. Selected harmonic elimination (SHE) PWM
4. Sinusoidal-pulse PWM (SPWM)
5. Harmonic Injected Modulation
6. Space vector-pulse PWM (SVPWM)

IV. SINE PULSE WIDTH MODULATION(SPWM)

The SPWM technique is based on the comparison of a carrier signal and a pure sinusoidal modulation signal. It was introduced by Schonung and Stemmler in 1964 as reported in (Kumar et al. 2008). The utilization rate of the DC voltage for traditional sinusoidal PWM is only 78:5% of the DC bus voltage, which is far less than that of the six-step wave (100%). Improving the utilization rate of the DC bus voltage has been a research focus in power electronics. The sinusoidal pulse-width modulation (SPWM) technique produces a sinusoidal waveform by filtering an output pulse waveform with varying width. A high switching frequency leads to a better filtered sinusoidal output waveform. The desired output voltage is achieved by varying the frequency and amplitude of a reference or modulating voltage.

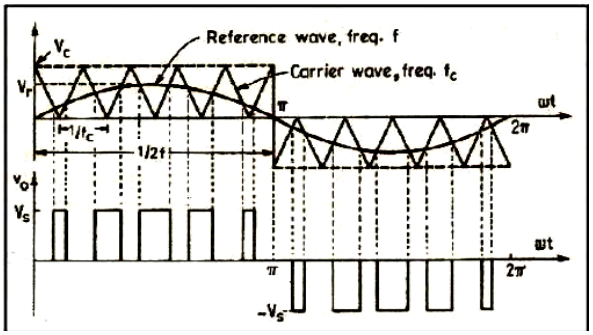

Fig. 5 Output voltage waveform with sinusoidal pulse modulation

The variations in the amplitude and frequency of the reference voltage change the pulse-width patterns of the output voltage but keep the sinusoidal modulation. When triangular carrier wave has its peak coincident with zero of the reference sinusoid, there are N=fc/2f pulses per half cycle; Fig. has five pulse. In case zero of the triangular wave of coincides with zero of the reference sinusoid, there are (N-1) pulses per half cycle.

V. SPACE VECTOR PULSE WIDTH MODULATION (SVPWM)

The space vector modulation (SVM) method is an advanced, computation-intensive PWM method and is possibly the best method among the all PWM techniques for variable-frequency drive application. Because of its superior performance characteristics, it has been finding wide spread application in recent years.

SVM is an algorithm for the control of pulse width modulation (PWM). It is used for the creation of alternating current (AC) waveforms; most commonly to drive three phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

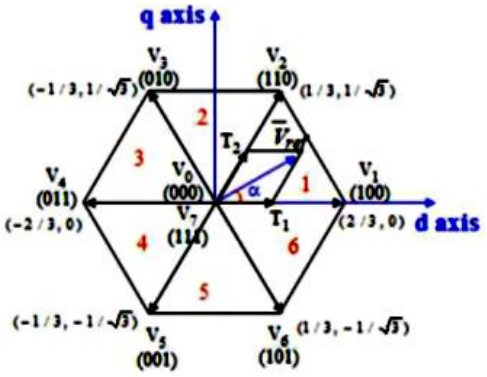

Fig. 6 Basic switching vectors and sectors

To implement space vector modulation a reference signal V_{ref} is sampled with a frequency fs (Ts = 1/fs). The reference signal may be generated from three separate phase references using the Clarke's transform. The reference vector is then synthesized using a combination of the two adjacent active switching vectors and one or both of the zero vectors. Various strategies of selecting the order of the vectors and which zero vector(s) to use exist. Strategy selection will affect the harmonic content and the switching losses. So Space Vector Modulation can be implemented by the following steps:

- Step 1. Determine V_d, V_q, Vref, and angle (α)
- Step 2. Determine time duration T1, T2, T0
- Step 3. Determine the switching time of each transistor of inverter.

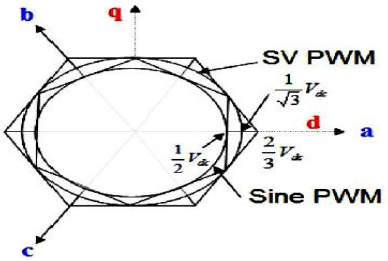

Fig.7 Locus Comparison of Maximum Linear Control Voltage in Sine PWM and SVPWM

A. Simulations And Result

Simulink model of svm for two level inverter

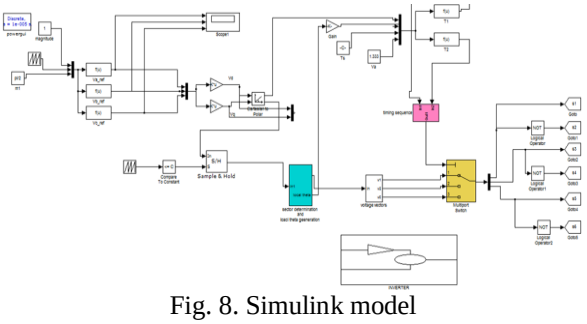

Fig. 8. Simulink model

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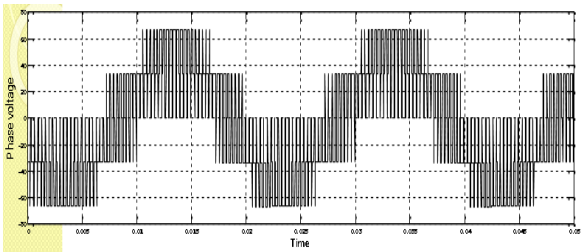
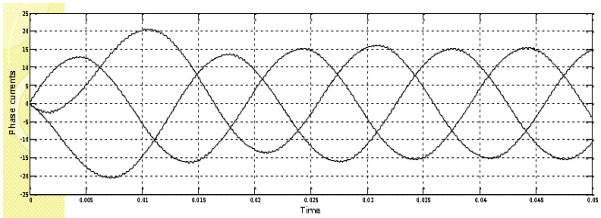
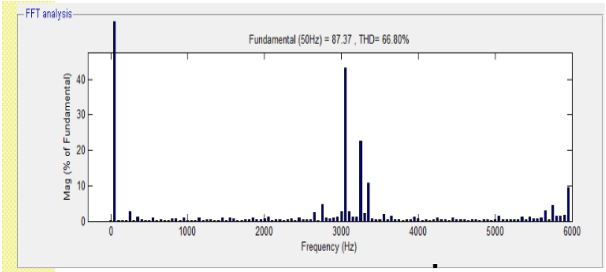


Waveform Of Phase Voltages Of Two Level Inverter



Load current waveform of two level inverter



FFT of line voltage of two level inverter

VI. CONCLUSION

Simulink model for the two techniques- SPWM and SVM (proposed technique) have been developed and tested in the MATLAB/Simulink environment. From the results obtained it is concluded that as the level of inverter increases the fundamental component increases and THD reduces.

On comparing the result of three, five and seven level inverters employing SVM and SPWM, SVM is found superior to SPWM in terms of fundamental and THD.
Simulation results of two-level SVM confirm that the amplitude of line to line voltage is as high as DC bus voltage in SVM technique. Among three switching state and four switching state technique, though THD of four switching inverter increases slightly, but lower order harmonics are reduced and the current harmonics are much less in inverter employing SVM with four switching states.

TABLE 1

Sr.No.	Harmonic order	Using three switches	Using four Switches
1.	5	2.60	1.14
2.	7	1.20	0.86

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BIOGRAPHY

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